REMARKS

Claims 2, 6 and 9-12 have been cancelled. Thus, Claims 1, 3-5 and 7-8 are currently pending in the present application, of which Claims 1 and 5 have been amended.

Claims 1 and 5 have been amended as suggested by the Examiner. Thus, the claim objections are believed to be overcome.

Rejection under 35 U.S.C. § 101

Claims 2, 6 and 10 were rejected under 35 U.S.C. § 101 because the claimed invention is not supported by either a substantial asserted utility or a well-established utility. Claims 2, 6 and 10 have been cancelled; thus, the § 101 rejection is deemed moot.

Rejection under 35 U.S.C. § 112

Claims 2, 6 and 10 were rejected under 35 U.S.C. § 112, first paragraph, because the claimed invention is not supported by either a substantial asserted utility or a well-established utility. Claims 2, 6 and 10 have been cancelled; thus, the § 112 rejection is deemed moot.

Rejection under 35 U.S.C. § 103

Claims 1, 4-5, 8-9 and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Devlin et al.* (US 6,710,621) in view of *Gheewala* (US 6,091,090). Applicant respectfully traverses such rejection insofar to it might apply to the claims amended herein.

Amended Claim 1 (and similarly Claim 5) now recites "grouping circuit macros of like power supply voltages into respective logic blocks" and "synthesizing said logic blocks using sub-libraries corresponding to power supply voltages for said logic blocks."

On page 4 of the Office Action, the Examiner asserts that the claimed grouping and synthesizing steps are disclosed by *Devlin* in Figure 2 and col. 2, lines 56 - 59. The Examiner also asserts that *Devlin* discloses "like power supply voltages are grouped into respective logic blocks." In col. 2, lines 56 - 59, *Devlin* simply states that

> modern FPGAs such as Virtex-E require multiple power supply voltage. As well as the "core" power supply voltage groups or "banks" of I/O pins can operate independently at different voltage levels.

The above-mentioned statements describe what's shown in Figure 2, which is each I/O pin bank being connected to two different voltage supplies. Since *Devlin* teaches that two different voltage supplies can be connected to each I/O pin bank, *Devlin* does not teach or suggest "grouping circuit macros of like power supply voltages into respective logic blocks" (emphasis added), as claimed. Since *Devlin* does not teach or suggest the claimed grouping step, *Devlin* also does not teach or suggest the claimed synthesizing step either.

Claim 1 also recites "reserving metal layer M1 for power supply bus when developing a bus structure of an ASIC device image." On page 4 of the Office Action, the Examiner states that the claimed reserving step is not taught or suggested by *Devlin*; however, the Examiner asserts that the claimed reserving step is disclosed by *Gheewala* in col. 1, line 65 - col. 2, line 3.

In col. 1, lines 24-29, *Gheewala* teaches that macro cells are commonly used elements such as NAND gates, NOR gates, flip-flops, etc., and the macro cells may be interconnected in a variety of ways to perform desired functions. *Gheewala*'s macro cells are at gates level, which is at a lower level than the *Devlin*'s "core" logic and "banks" of I/O pins. Thus, the teachings of *Gheewala* and *Devlin* cannot be combined without further suggestion from either one of the cited references. Because the cited references, whether considered separately or in combination, do not teach or suggest all the features of the claimed invention, the § 103 rejection is believed to be overcome.

CONCLUSION

Claims 1, 3-5 and 7-8 are currently pending in the present application. For the reasons stated above, Applicant believes independent Claims 1 and 5, and all their respective dependent claims are distinguished over the cited references under § 103, and should be in condition for allowance. The remaining prior art cited by the Examiner, but not relied upon, has been reviewed and is not believed to show or suggest the claimed invention.

No fee or extension of time is believed to be necessary; however, in the event that any fee or extension of time is required for the prosecution of the present application, please charge it against BAE Systems Deposit Account No. 19-0130.

Respectfully submitted,

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